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A High Efficiency Doherty Amplifier with Digital Predistortion for WiMAX

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This article describes a WiMAX power amplifier , which achieves high performance using the latest device technologies and design techniques

The Doherty amplifier architecture is a well known technique offering the potential to improve transmitter efficiency especially for signal protocols that exhibit high peak-to-average power ratios. Although the Doherty approach has significant efficiency advantages, it generally must be augmented with some form of correction or linearity enhancement in the full transmitter design. Wireless infrastructure applications have demanding linearity and spectral mask specifications. The latest WiMAX standards present a particular challenge with their combination of very high peak-to-average power ratios, 10 MHz or wider channel bandwidths and high linearity standards. This article demonstrates a 2.5-2.7 GHz Doherty amplifier that achieves, when augmented with digital predistortion, 8 watts of WiMAX average output power at greater than 47% efficiency, while satisfying demanding spectral mask specifications.

The appeal of the Doherty amplifier configuration is that it involves familiar core amplifier designs connected in a manner that maintains high efficiency over an extended input signal range. Doherty development has been energized by the latest generations of transistors and is well represented in recent literature [1-5]. Applying the Doherty approach to modern WiMAX signals can present unique challenges. In particular, WiMAX signals combine two challenging features: wide video bandwidth of 10 MHz or greater, and large peak-to-average ratios of 10 dB or greater. Additionally, the latest WiMAX standards require that the spectral emissions mask (SEM) at close offsets (1.5 MHz) be at least –45 dB. A typical amplifier (without correction) will exceed this level by 15 to 20 dB, resulting in a significant correction demand for the digital predistortion circuitry.

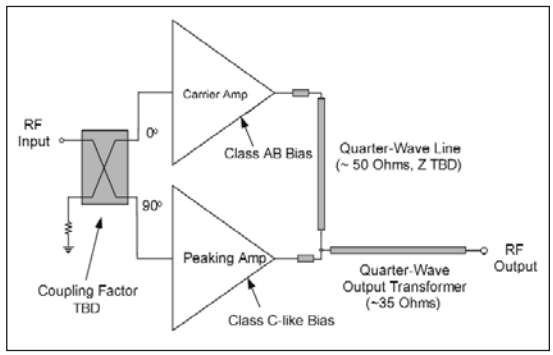

Figure 1 · A basic 2-way Doherty amplifier configuration.

The technologies applicable to this challenge have improved in three areas:

- Improved GaN HEMT transistors with reduced capacitances and trapping effects
- Improved digital predistortion subsystems and software
- Doherty circuit design refinements that reduce memory effects, increase gain and increase bandwidth.

This article focuses on the optimization of Doherty amplifier circuitry for WiMAX applications.

Amplifier Design Approach

Doherty amplifiers can be configured with 2-, 3- or N-way combinations [8, 9, 10]. The most commonly used Doherty architecture

involves two amplifiers, as shown in Figure 1. Adding additional branches can extend the power range over which high efficiency is maintained. However, the 2-amplifier approach is often preferred due to cost considerations (i.e., using fewer devices). Fortunately, there are multiple variables besides the number of branches that can be adjusted to optimize performance.

The Doherty block diagram (Fig. 1) is notable for its elegance and simplicity. What may not be apparent is that details of the design can result in large differences in performance. Operation is strongly influenced by the coupling factor of the input divider/coupler and by the biasing of the carrier and peaking amplifier stages. The "turn-on" of the peaking amplifier is dependent on both input power level and gate bias voltage, which in turn sets the low power efficiency and peak power capability of the configuration. The peaking amplifier allows the Doherty amplifier to respond to the high input levels of short duration by amplifying the signal peaks and dynamically changing the loading on the main amplifier.

The specific class of operation (Class A/B, Class B, Class C, Class F, inverse Class F, etc.) of each amplifier is also important. The two basic considerations for each stage are the bias conditions (biased on, or pinched off, and to what degree) and the fundamental and harmonic impedance terminations presented to the transistors. Previous papers on Doherty design have advocated particular classes of operation for the carrier and peaking amplifiers [6]. The approach described in this article was to start with a waveform-engineered design, in which the "stand-alone" stage (i.e., outside the Doherty environment) was optimized in a 50-ohm system. Then the biases were adjusted for carrier and peaking functions and the stages were inserted into the Doherty configuration. Waveform engineering [7] was used to maximize

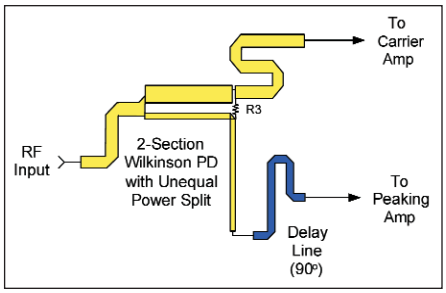

Figure 2 · Schematic of an unequal power divider for Doherty application.

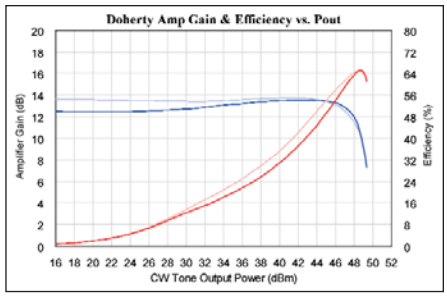

Figure 3 · Simulated gain and efficiency vs. CW output power for two input couplers. Dark trace is for 3 dB (equal) coupling. Light trace is for approximately 1.8/4.7 dB coupling (more power to carrier amplifier versus peaking amplifier).

amplifier efficiency over a power range from 10 dB backoff to peak (saturated) output level.

Series matching elements of each stage were modified to reduce electrical length from the transistor to the combining node, and harmonic terminations were adjusted to optimize the designs under Doherty operation.

It has been our experience that circuit modifications required after insertion into the Doherty configuration have been minimal for the input matching circuits, but substantial for the output circuits. Inserting the preferred stage designs as carrier and peaking stages (optimized for stand-alone operation in a 50-ohm environment), without further optimization, results in considerable performance sacrifice. Of course, this approach is predicated on the availability of accurate non-linear transistor models and CAD tools such as the Microwave Office non-linear (harmonic balance) simulator.

The potential for correction using digital predistortion is improved by two additional features: (1) maximizing the RF bandwidth of the Doherty amplifier, and (2) increasing the video bandwidth by minimizing the drain bias feed inductance.

Sensitivity to Input Divider Coupling Factor and Stage Bias

The input power divider for the design is a variation of a 2-section Wilkinson divider (Fig. 2), with the second isolation resistor omitted because of layout constraints. This divider maintains a reasonable level of isolation, while being more compact than if it were extended to accommodate a second resistor. The delay line is added to provide the desired quadrature relationship of the two outputs. The coupling is determined by the relative line widths (impedances) of the two branches. The divider block could be further compacted by substituting a custom coupled-line design with over-coupling (possibly requiring a multi-layer printed circuit board (PCB), or a custom component). The approach employed here is realizable with a single layer PCB, and it allows considerable flexibility in setting the coupling ratio.

The Doherty amplifier performance was simulated for various input couplers and peaking amplifier bias levels. All simulations are at 2.6 GHz with a drain supply voltage of +28 volts DC. The devices are Cree CGH27030F GaN HEMT transistors.

The plot of Figure 3 shows the result of simulations for two Doherty amplifiers that are identical except for the input couplers. The dark trace is for equal power to both the carrier and peaking amplifiers. The light trace is for an unequal power divider (approximately 1.8/4.7 dB coupling) in which approximately 3 dB more

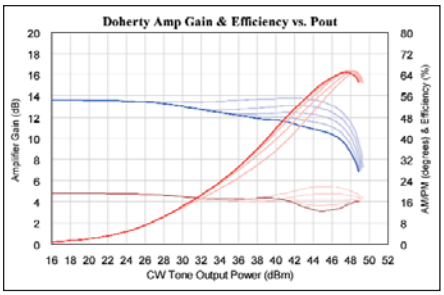

Figure 4 · Simulated gain and efficiency versus CW output power, for different gate bias voltages for the peaking amplifier (1.8/4.7 dB input coupler). The dark trace is for V_{gs} = –5 volts. Voltage steps are 0.5 V.

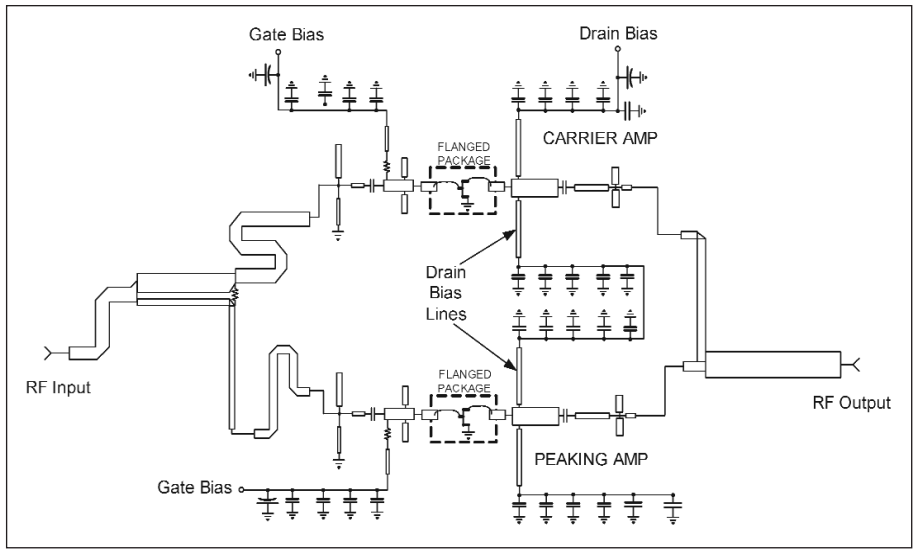

Figure 5 · Doherty amplifier schematic.

power is directed to the carrier amplifier than to the peaking amplifier. The unequal coupling case supports significantly higher efficiency in the backoff power range (a 4.3% efficiency improvement at 10 dB below the peak power is predicted as well as more uniform gain as a function of output power). The Doherty amplifier used for this simulation is not strictly an efficiency-optimized amplifier—rather, it was optimized with equal emphasis on peak power, linearity and efficiency.

The simulations of Figure 4 are for the unequal input divider, with the gate bias voltage to the peaking amplifier varied from –3.0 to –5.0 volts. The more negative the gate voltage, the later the peaking amplifier turns on as power is increased. These simulations suggest that increasing the gate voltage (more negative) improves efficiency in backoff, progressively introduces more AM/AM, but—surprisingly—also can decrease the AM/PM. The AM/PM is predicted to be very low at the optimum gate bias. These simulations are for CW signals, and the results will differ for dynamic WiMAX signals. An improvement in efficiency and linearity is observed with increasing gate voltage for the hardware under WiMAX drive signals. It is also worth noting that these plots (Fig. 4) suggest that it is fruitful to examine the effectiveness of digital predistortion for various peaking amplifier gate bias levels.

Amplifier Schematic and Drain Bias Design

The 2.5-2.7 GHz Doherty amplifier schematic is shown in Figure 5. The input and output matching circuits of the carrier and peaking amplifier stages use conventional matching circuitry. The open circuit stubs on the input and output are placed at critical junctions where they have the desired impact on source and load impedances. The output circuit includes two drain bias lines per device, in order to reduce video impedance. Additionally, the length of these bias lines is chosen to assist in positioning the load presented to the devices at second harmonic frequencies. The impedance at the second harmonics is approximately a short circuit (as a stand-alone subcircuit in a 50-ohm system), although the precise angle (bias line length) is adjusted during simulation of the full Doherty amplifier.

The motivation for limiting the inductance of the drain feed lines is to reduce memory effects, which can be exacerbated by bias circuits. The output circuit (including bias elements) impedance at video frequencies is also simulated. For this circuit, the magnitude of the impedance presented to the drain increases monotonically from a few milliohms at 100 kHz to 200 milliohms at 10 MHz, and approximately 1 ohm at 50 MHz (dominated by the effective inductance of the bias feeds).

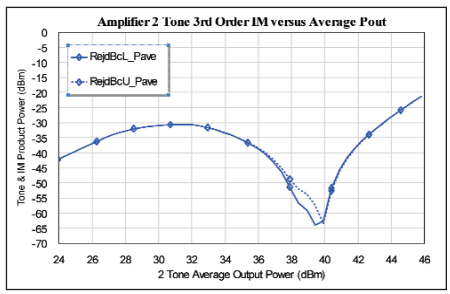

Figure 6 · Simulated 2-tone intermodulation products versus output power level (tone separation of 1 MHz).

The typical 3rd order two tone intermodulation products as a function of output power for the Doherty amplifier design are also examined as these relate directly to the error vector magnitude (EVM) and relative constellation error (RCE) of the amplifier when driven by WiMAX signals. The simulations of Figure 6 demonstrate a typical "back-off hill"

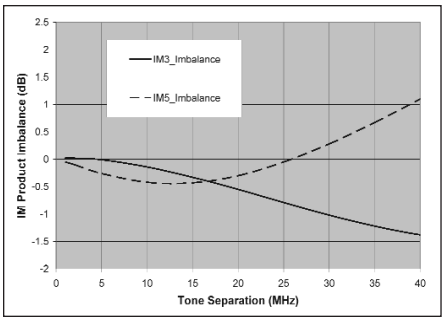

Figure 7 · Simulated 2-tone IM products imbalance versus frequency separation of tones (P_{out} = +32 dBm).

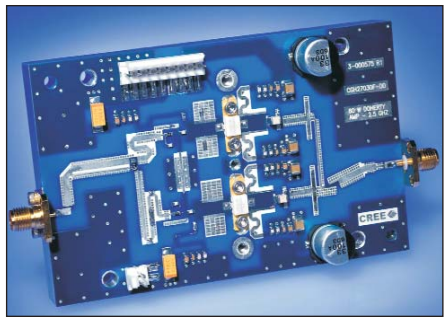

Figure 8 · The 2.5-2.7 GHz Doherty amplifier with two 30W GaN HEMTs PCB size is 2.5 × 4.0 inches.

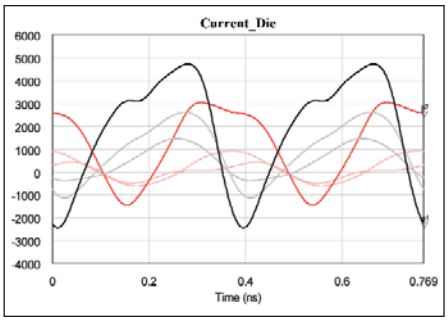

Figure 9 · Simulation of drain currents at the carrier (black) and peaking (red) transistors with single-tone P_{out} = 36, 42 and 48 dBm.

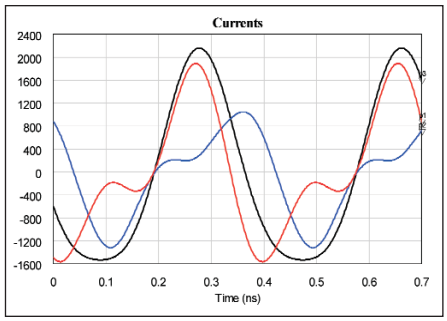

Figure 10 · Simulation of currents at Doherty output combiner node, single-tone P_{out} = 48 dBm; black = output arm, red = carrier arm, blue = peaking arm.

in intermodulation distortion at about +32 dBm average output. Note that upper and lower IM products (at frequencies $2F_2–F_1$ and $2F_1–F_2$) are nearly equal except in the "sweet spot" power range, for this case of a 1 MHz difference between F_1 and F_2. The imbalance between the upper and lower IM products is a function of several parameters, including the impedances presented to the devices at fundamental, harmonic, sum and difference frequencies. The bias circuit impacts the impedances at the difference (video) frequencies. It is illustrative to simulate the 2-tone IM rejection at the hill power (+32 dBm) versus frequency of separation between the tones. The inequality of IM products versus tone separation differs depending on power level, and the plot of Figure 7 is for a +32 dBm output level (illustrative of the hill region). This simulation shows that the imbalance of 3rd and 5th order intermodulation tones (at +32 dBm output) is less than 0.5 dB for tone separations to 18 MHz. This is significant for applications involving 10 MHz wide WiMAX signals.

The output matching structures of the carrier and peaking amplifiers were adjusted while examining both the 2-tone IM rejection and the single tone gain and efficiency versus output power. Critical circuit elements included the matching elements at the fundamental frequency, as well as the bias lines for harmonic matching. All of these elements were adjusted after integration into the Doherty configuration (relative to the values in a stand alone 50-ohm environment). The width (impedance) of the quarter wave line connecting the carrier and peaking amplifier outputs is a sensitive parameter, as are the open circuit stubs near this line. The output transformer was found to exhibit relatively low sensitivity.

The Doherty amplifier is shown Figure 8. The devices are Cree CGH27030F GaN HEMT transistors. The printed circuit board is Rogers RO4350B material with 0.5 mm thickness. The amplifier construction is conventional, using commonly available components and materials. Only a few of the tuning pads were used in the prototype alignment, as the transistor modeling and simulations proved to be accurate.

Time Domain Simulations of Doherty Operation

The Doherty amplifier was designed from a frequency domain perspective, modifying elements to improve efficiency, 2-tone linearity, and peak power. This process involved simulations commonly used by microwave engineers, including CW gain and efficiency versus output power, and two tone IM distortion versus output power. However it is also informative to examine the resulting amplifier from the time domain perspective. The plots of Figures 9 and 10 are of currents at critical nodes in the circuit (F = 2.6 GHz, V_{ds} = +28V, I_{dq} = 170 mA for the carrier amplifier and V_{gs} = –4.0 volts for the peaking amplifier).

The simulations resulting in Figure 9 show the drain currents at the two transistors, for three output power levels of +36 dBm, +42 dBm and +48 dBm. Recall that the drive to the peaking amplifier is offset (relative to that to the carrier amplifier) by 90 degrees due to the delay line in the Doherty circuitry. The peak transistor currents contribute strongly only at the highest output power. It is interesting to note the relatively non-sinusoidal shape of the individual waveforms. The simulated currents are at the die drain pads, and the

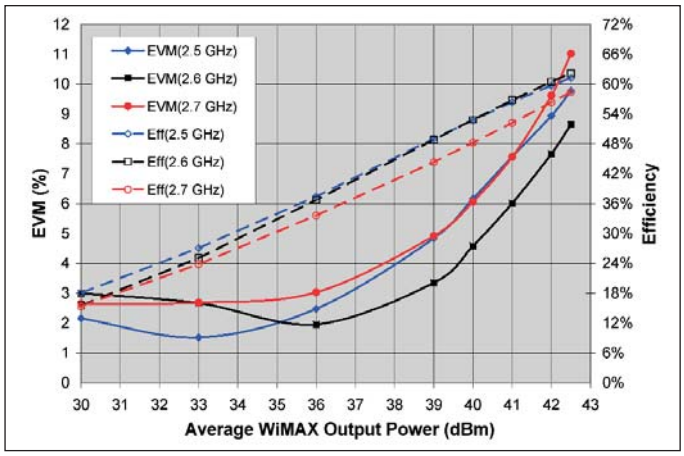

Figure 12 · Measured Doherty amplifier EVM and efficiency vs. WiMAX P_{out} (without predistortion).

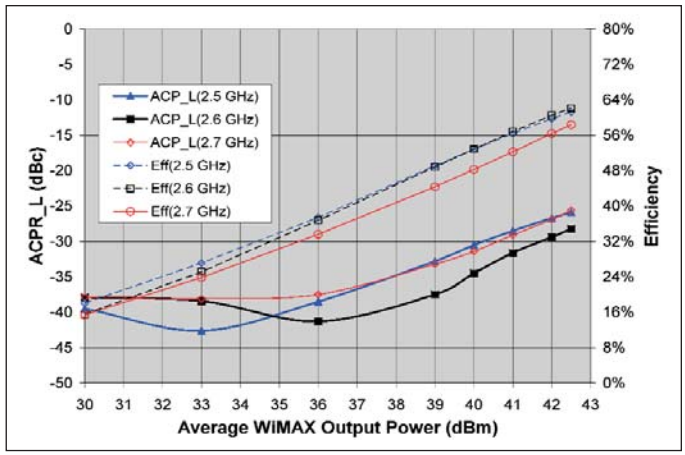

Figure 13 · Measured Doherty amplifier ACPR and efficiency vs. WiMAX P_{out} (without predistortion).

intrinsic capacitances of these devices are clearly important. These waveforms suggest some sort of Class J operation as defined by Cripps [7]. These current simulations show that the higher order (3rd, 4th, etc.) harmonic terminations on the amplifier outputs are non-ideal for efficiency optimization since the waveforms are not "squared off," but are rather soft in their transitions. This is due to the emphasis on (uncorrected) linearity during circuit optimization.

The currents shown in Figure 10 are those flowing into the Doherty combining node for the main and peaking amplifiers, and exiting the node for the output arm at +48 dBm output power. The output arm current equals the sum of the main and peaking arm currents. The currents add constructively to produce a near-

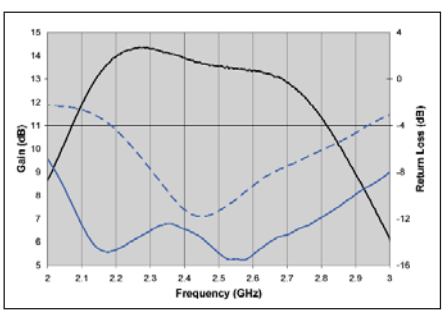

Figure 11 · Measured small-signal gain and input and output return loss versus frequency (output return loss is dashed line).

ly sinusoidal waveform. It is interesting to observe that the role of the peaking amplifier appears to be more a matter of complex waveform synthesis, as opposed to the more elementary view involving Class C like current pulses.

Measured Amplifier Performance

The design was optimized for linearity and efficiency over the 2.5-2.7 GHz range to support a number of possible WiMAX frequencies. The small signal bandwidth exceeds this limited range as shown in Figure 11. Gain is nominally 13 dB and input return loss is typically 14 dB.

The efficiency and linearity of the final amplifier were evaluated using a 10 MHz wide WiMAX signal compliant to 802.16e-2005. The key linearity parameters for this modulation scheme are error vector magnitude (EVM), as shown in Figure 12, and spectral emissions mask (SEM). The spectral mask was measured using a 10 MHz wide integration bandwidth in the adjacent channel, as shown in Figure 13, at 2.5, 2.6 and 2.7 GHz. The performance is optimum at 2.6 GHz with trade-offs in linearity at the band edges. Efficiency versus output power is flat over 2.5 to 2.6 GHz dropping by approximately 5% at 2.7 GHz. It is clear that single frequency designs (optimized at either 2.5 or 2.7 GHz, not 2.6 GHz) would offer the potential for incrementally higher efficiency.

Description of WiMAX Protocol and Digital Predistorter Design

The digital predistortion (DPD) test-bed used for correction of this Doherty amplifier was provided by Optichron. The test-bed used is the base-band development board with the OP4400 chipset. A block diagram of the system is shown in Figure 14. The WiMAX signal, which is a fully compliant 802.16e-2005 signal, is used as a stimulus to the test-bed. This signal is generated using Rohde and Schwarz AMIQ equipment and applied to the test-bed in digital I and Q format. When setting up the test-bed the signal is first passed through the OP4400 chipset with no correction applied. This allows the performance of the uncorrected amplifier to be observed. The digital signal is fed to a Texas Instruments TSW3003 upconverter. The up-converted signal level at the output of the radio board is approximately –10 dBm and therefore needs to be amplified to be able to drive the Doherty amplifier to the required power levels. It should be noted that this amplifier is located within the predistortion loop (labeled in Figure 14 as the "Driving Amp"), which means that it's performance,

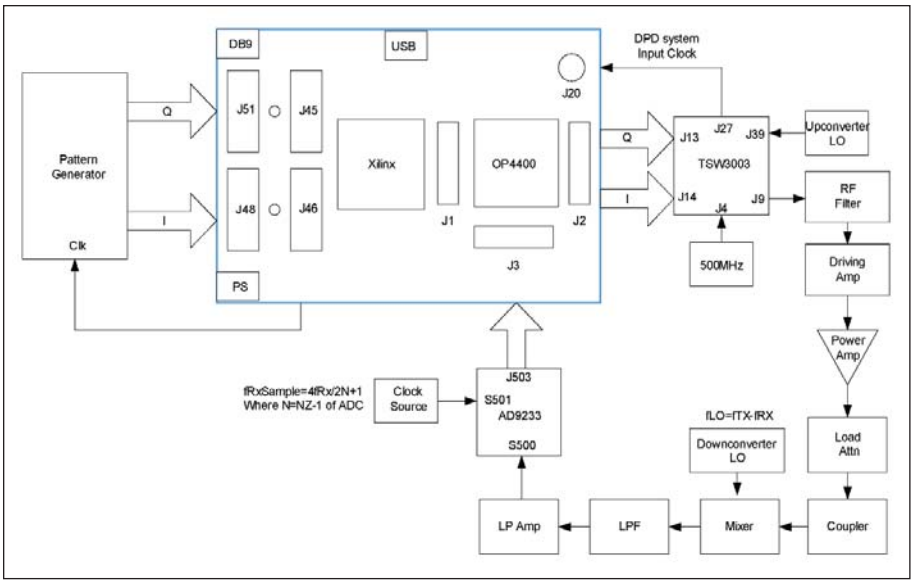

Figure 14 · Digital predistortion test-bed using Optichron OP4400 chipset.

albeit extremely linear, is also being corrected by the test-bed. The resulting modulated signal is then applied to the amplifier under test which creates some level of unwanted distortion. The output signal is sampled and downconverted using a commercially available Mini Circuits mixer. The IF signal is then processed by an Analog Devices analog to digital converter (AD9233). The resulting digital representation of the output signal is then processed by the Optichron OP4400 chipset. At this point a digitally predistorted signal is then reapplied to the amplifier under test in real time. The option exists within the test-bed's software controls for the user to decide whether to use a simple memoryless algorithm or whether to choose a more complex algorithm which would help correct amplifiers with strong memory effects.

It was found that, at low average power levels, the memoryless algorithm was sufficient to correct the non-linearities of the Doherty amplifier down to the system noise floor associated with the 50 dB gain driver amplifier. This was somewhat compensated with the use of attenuation at the output of that amplifier. At the maximum output power both algorithms were needed due to the large amounts of clipping occurring at the peaks of the WiMAX signal. At 8 watts average output power the crests were being clipped from their theoretical level of 100 watts by the peak capability of the Doherty amplifier which was estimated to be about 60 watts. This equates to more than 2 dB compression assuming that the peak-to-average power ratio (PAPR) was not increased by the digital predistortion algorithm!

The required SEM at 1.5 MHz offset from the edge of the signal is –45 dB. This specification was met at 8 watts of average output power and at 47% DC-RF efficiency for a WiMAX 10 MHz channel bandwidth signal with 11 dB peak-to-average ratio, as shown in Figure 15 . The correction in SEM with the Optichron OP4400 DPD test-bed was 17 dB. The plot of Figure 16 shows that such excellent correction is maintained across frequency (2.5 and 2.655 GHz) as well as with average output power. It can be seen that the distortion products of a Doherty amplifier are relatively

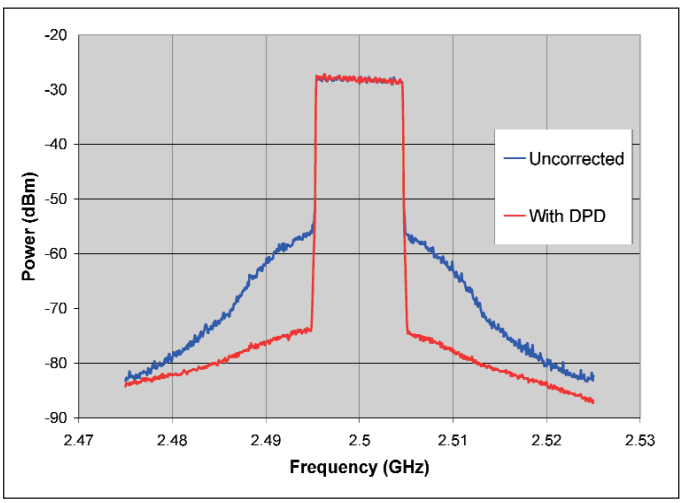

Figure 15 · Doherty amplifier spectral mask, with and without DPD correction (F = 2.5 GHz, P_{ave} = 8 watts, V_{supply} = +28 V, I = 600 mA, 48% DC-RF efficiency).

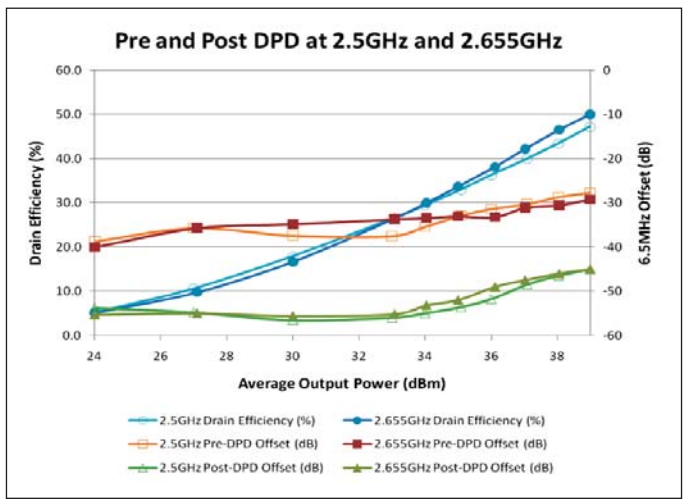

Figure 16 · Doherty amplifier spectral mask vs. average output power, with and without DPD correction (F = 2.5, 2.655 GHz, V_{supply} = +28 V).

high when the output power is backed off quite heavily from the maximum average output power. The DPD system, however, is able to correct down to the system noise floor with better than 20 dB correction over a wide dynamic range.

These results demonstrate the feasibility of a compact, high efficiency design for WiMAX transmitters at 2.5 or 2.7 GHz with up to 8 watts average output power.

Summary and Conclusions

A number of design considerations for Doherty amplifiers using GaN HEMT transistors in the 2.5-2.7 GHz bands have been presented. The critical roles of the input coupler and peaking amplifier bias point were described, as well as the rationale for input divider design and the choice of amplifier bias. The importance of bias circuit design and the evaluation of such circuits were also covered. The design optimization process was described, including the key parameters and tradeoffs involved. Finally, the effectiveness of digital predistortion for this Doherty amplifier with GaN HEMT transistors was demonstrated. The result was a fully specification compliant WiMAX amplifier with 8 watts average output level at an extraordinary 47% efficiency.

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Ray Pengelly gained his BSc. and MSc. degrees from Southampton University, England in 1969 and 1973, respectively. Since August 1999, Ray has been employed by Cree Inc. Initially, he was the General Manager for Cree Microwave responsible for bringing Cree's wide bandgap transistor technology to the commercial marketplace. On the acquisition of UltraRF, Sunnyvale in 2001, he became Chief Technical Officer enabling his skills in microwave semiconductor technology, based on 30 years of experience, to be utilized. From September 2005 he became responsible for new business development of wide bandgap technologies for RF and microwave applications for Cree in Durham, NC and most recently has been involved with the release of GaN HEMT transistors and ICs for general purpose and telecommunications applications. Ray has written over 100 technical papers, 4 technical books, holds 12 patents and is a Fellow of the IET and Senior Member of the IEEE.

Jim Crescenzi received the BS degree at UC Berkeley in 1961 and the MS and PhD degrees at the University of Colorado in 1962 and 1969. He founded Central Coast Microwave Design in 2005, where he provides consulting services primarily for microwave power amplifiers and subsystems. Jim is a Life Fellow of the IEEE for contributions to the development of microwave amplifiers, integrated circuit technology, and miniature receivers for defense applications. He can be reached at jcrescenzi@gmail.com.